TVS Placement
The Critical Path to the Leading Edge

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Reverse avalanche transient suppressors have excellent turn-on characteristics. Typically these devices turn on in sub-nano second time frames. When protecting small geometry integrated circuits it is important to “catch” the leading edge of transient surges with very steep rise times.

Parasitic inductance in the circuit configuration and component layout inhibit the suppressor’s ability to catch the leading edge of an ESD surge or other very fast pulses.

The suppressor should be as physically close to the vulnerable component’s ground return as possible (see Figure 1). The lower the parasitic inductance between the ground plane of the component to be protected and the TVS, the more effective the suppressor will be.

ESD can have rise times as steep as 64 kV/ms or 30 kA/ms. Though the total energy is minimal, the peak is easily capable of rupturing the gate oxide at the input stage of a data transceiver chip. Fortunately it is possible to use the parasitic inductance of the P.C.B. to your advantage.

In Figure 2 it is shown that the inductance inherent in the P.C.B. conductive traces can be used to slow down the leading edge of an incoming transient, thereby reducing the importance of the inductance between the TVS diode element and the critical ground path.

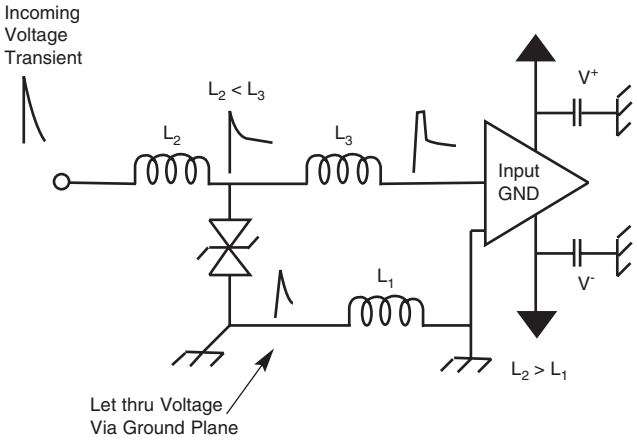

Figure 1.

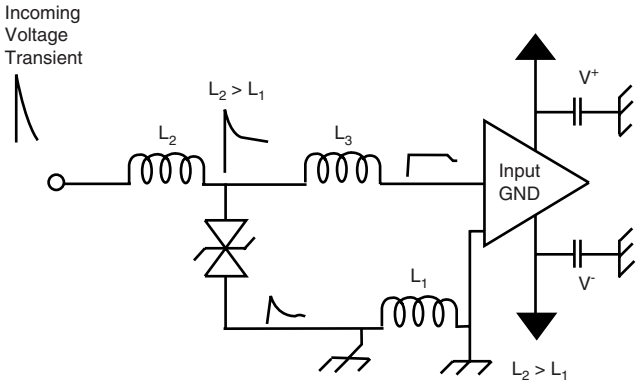

Figure 2.

For both Figure 1 and Figure 2:

L_1 = inductance of ground plane
L_2 = inductance of P.C.B. trace from input to TVS
L_3 = inductance of P.C.B. trace from TVS to transceiver into pin